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Bharatiya Vidya Bhavan's

Sardar Patel College of Engineering



Semester: VI

MASTER FILE

(A Government Aided Autonomous Institute) Munshi Nagar, Andheri (West), Mumbai – 400058.

End Sem Re - Exam

June 2017

Q. P. Code:

Max. Marks: 100

Duration: 3 hr

Class: Third Year

Program: Electrical Engineering

Name of the Course: Elective - VLSI

Course Code: BTE332

Instructions:

• Question One is Compulsory.

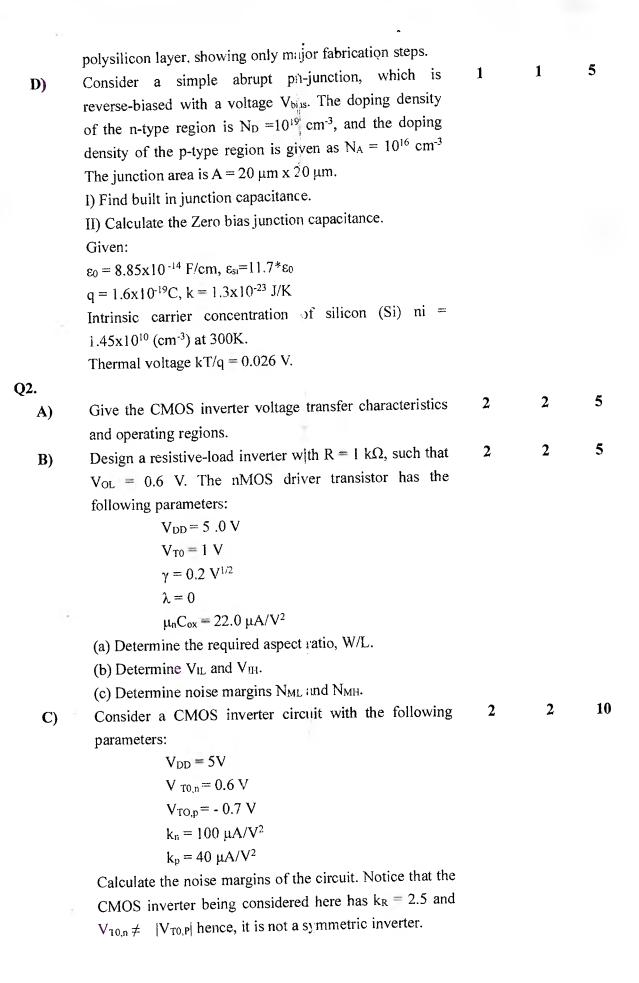
Solve any four of remaining six questions.

Illustrate your answers with neat sketches wherever necessary.

Assume suitable data if required.

Preferably, write the answers in sequential order.

Question No.		Modul e Numbe	Cour se Outc	Max. Mark s	
		r	ome		
Q1. A)	Compare the two technology scaling methods, namely, (i) the constant electric-field scaling and (ii) the constant power-supply voltage scaling. In particular, show analytically by using equations how the delay time, power dissipation, and power density are affected in	1	1	5	
В)	terms of the scaling factor, S. Compare BJT, NMOS and CMOS technology.	1	1	5	
C)	Explain simplified process sequence for the fabrication of the n-well CMOS integrated circuit with a single	1	1	5	



Q.3		2	2	5
A)	Draw the circuit and layout of CMOS NAND2 gate.	2	3	5
B)	Define: i) Pseudo-nMOS gate, ii) transmission gate.	3	3	3
,	Implement two input multiplexer using CMOS			
	transmission gate.	2	3	5
C) ·	Write short note on SR latch circuit.	3	3	5
D)	Write short note pass transistor logic	3	3	•
Q.4		4	3	5
A)	Give the classification of semiconductor memories.	4	3	J
·	Draw typical random access memory array organization.	4	3	10
B)	Design a 4-bit X 4-bit NOR based ROM array to store	4	3	10
,	following data stream. Also write its column and rows			
	combination.			
	Data: 1001			
	1110			
	0110			
	1001			
	Draw layout for circuit designed.		•	5
C)	Discuss the operation of resistive-load SRAM Cell.	4	3	3
Q.5			3	10
A)	Discuss the operation of three transistor DRAM Cell.	4	3	5
B)	Explain Partial-product generation.	5	3	5
C)	Write short note on barrel shifter.	5	3	J
Q.6			4	5
A)	What is clock skew? What are the sources of clock	6	4	5
	skew? How it can be overcome?			_
B)	Explain clock system architecture.	6	4	5
C)	Explain in detail global clock generator of clock system.	6	4	5
D)	Comment on the advantages and disadvantages of	6	4	5
	H-trees and clock grids. How does the hybrid tree/grid			
	improve on a standard grid?			
Q.7		_	4	
A)	Explain how an electrostatic discharge event could cause	7	4	5
	latchup on a CMOS chip	_		
B)	Define:	7	4	5
	A) VDD & GND pads.			
	B) Input and Output Pads.			
	C) Bidirectional pads.			

D) Analog pads.

Draw bidirectional pad circuitry.

C) Write short note on Elmore delay. 7 4 5

D) Define crosstalk. What are the effect of crosstalk delay 7 4 5 and crosstalk noise on interconnect.